

Claims:

1. A computer system, comprising:
2 a first processor;
3 a second processor; and
4 a direct memory access (DMA) engine capable of being executed by one of the first and
5 second processors, the DMA engine capable of transferring data between one or more resources
6 in the computer system.

1 2. The system of Claim 1, wherein the direct memory access engine further
2 comprises one or more instructions being executed by one of the first and second processors that
3 transfer data between the resources.

1 3. The system of Claim 2, wherein the resources comprise one or more of static
2 random access memory, dynamic random access memory and one or more hardware buffers that
3 are capable of interfacing with one or more peripheral devices.

1 4. The system of Claim 3, wherein the one or more hardware buffers, in combination
2 with the DMA engine, permit the one or more peripherals to access the memory directly.

1 5. The system of Claim 3, wherein the instructions further comprise a store multiple
2 data instruction and a load multiple data instruction wherein the load multiple data instruction
3 loads data from multiple locations in one of the hardware buffers into multiple locations in the
4 internal registers in the processor executing the DMA engine instructions and wherein the store
5 multiple data instruction transfers the data from multiple locations in the internal registers into
6 multiple locations in a memory.

1 6. A computer implemented direct memory access apparatus that operates in a
2 computer system having two or more processors, the apparatus comprising:
3 a load multiple data instruction capable of being executed by a processor in the computer
4 system for loading data from multiple locations in a resource into multiple locations in an
5 internal register in the processor; and
6 a store multiple data instruction capable of being executed by the processor in the
7 computer system for storing data from multiple locations in the internal registers in the processor
8 into multiple locations in a memory.

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1 7. The apparatus of Claim 6, wherein the resources comprise one or more of static
2 random access memory, dynamic random access memory and one or more hardware buffers that
3 are capable of interfacing with one or more peripheral devices.

1 8. The apparatus of Claim 7, wherein the one or more hardware buffers, in
2 combination with the DMA engine, permit the one or more peripherals to access the memory
3 directly.

1 9. The apparatus of Claim 8, wherein the instructions further comprise a store
2 multiple data instruction and a load multiple data instruction wherein the load multiple data
3 instruction loads data from multiple locations in one of the hardware buffers into multiple
4 locations in the internal registers in the processor executing the DMA engine instructions and
5 wherein the store multiple data instruction transfers the data from multiple locations in the
6 internal registers into multiple locations in a memory.

1 10. A computer implemented direct memory access apparatus that operates in a
2 computer system having two or more processors, the apparatus comprising:

3 a load multiple data instruction capable of being executed by a processor in the computer
4 system for loading data from multiple locations in a resource into multiple locations in an
5 internal register in the processor; and

6 a store multiple data instruction capable of being executed by the processor in the
7 computer system for storing data from multiple locations in the internal registers in the processor
8 into multiple locations in a memory; and

9 a data buffer FIFO capable of accepting multiple data transfers to and from any of its
10 alias addresses.